## IN THE CLAIMS

1-2. (Canceled)

3. (Original) The method of claim 7, wherein depositing a seed layer includes depositing a seed layer using a physical vapor deposition process.

4. (Canceled)

5. (Original) The method of claim 7, wherein depositing a layer of copper using electroless plating includes filling the number of via holes to a top surface of the photoresist layer.

6. (Canceled)

7. (Currently Amended) A method for forming vias on a substrate, comprising:

depositing a seed layer including a thin film of Palladium (Pd) or Copper (Cu) having a thickness of less than 15 nanometers (nm) on a semiconductor substrate;

depositing a patterned photoresist layer over the seed layer, wherein depositing the patterned photoresist layer defines a number of via holes opening to the seed layer;

depositing a layer of copper over the seed layer using electroless plating; and

removing the photoresist layer and exposed portions of the seed layer using oxygen plasma ashing.

8. (Previously Presented) A method for forming vias on a substrate, comprising:

depositing a seed layer including a thin film of Palladium (Pd) or Copper (Cu)having a discontinuous island structure on a semiconductor substrate using a sputtering deposition technique;

depositing a patterned photoresist layer over the seed layer, wherein depositing the patterned photoresist layer defines a number of via holes opening to the seed layer;

depositing a layer of copper over the seed layer using electroless plating.

9. (Original) The method of claim 8, wherein depositing a first seed layer having a discontinuous island structure includes a discontinuous island structure having a thickness of less than 15 nanometers (nm).

10. (Previously Presented) The method of claim 8, wherein depositing a layer of copper over the seed layer includes forming a number of copper structures, wherein copper structures are formed on the seed layer but not on the patterned photoresist layer.

11. (Previously Presented) The method of claim 10, wherein forming a number of copper structures includes filling the number of via holes to a top surface of the patterned photoresist layer.

12. (Original) The method of claim 8, wherein the method further includes removing the photoresist layer using oxygen plasma ashing.

13. (Previously Presented) A method for forming copper vias and a first metal layer, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a semiconductor substrate;

depositing a first patterned photoresist layer, wherein depositing the first patterned photoresist layer defines a first number of via holes above the first seed layer;

forming a first layer of copper using electroless plating, wherein forming the first layer of copper vias using electroless plating includes filling the first number of via holes to a top surface of the first patterned photoresist layer;

depositing a second seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the first layer of copper vias and the top surface of the photoresist layer;

depositing a second patterned photoresist layer, wherein depositing the second patterned photoresist layer defines a second number of conductor line openings above the second seed layer; and

forming a second layer of copper using electroless plating, wherein depositing a second layer of copper using electroless plating includes filling the second number of conductor line openings to a top surface of the second patterned photoresist layer.

14. (Original) The method of claim 13, wherein depositing a first seed layer includes depositing a first seed layer having a discontinuous island structure.

15. (Original) The method of claim 13, wherein depositing a first seed layer includes depositing a first seed layer using an evaporation deposition technique.

16. (Previously Presented) The method of claim 13, wherein forming a first layer of copper using electroless plating includes forming a first number of copper vias, wherein the first copper vias are formed on the first seed layer but not on the first patterned photoresist layer.

17. (Original) The method of claim 13, wherein depositing the second seed layer includes depositing the second seed layer using a physical vapor deposition process.

18. (Original) The method of claim 13, wherein depositing a second patterned photoresist layer includes depositing a second patterned photoresist layer which has a thickness which is less that a thickness of the first patterned photoresist layer.

19. (Previously Presented) The method of claim 13, wherein depositing the second patterned photoresist layer which defines a second number of conductor line openings includes a third number of first level metal line openings.

20. (Currently Amended) A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer on a semiconductor substrate;

patterning a first photoresist layer over the first seed layer to define a first number of via holes opening to the first seed layer;

forming a first level of copper vias in the first number of via holes using electroless plating to a top surface of the first photoresist layer;

depositing a second seed layer on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a second number of conductor line openings to the second seed layer;

forming a first level of conductor lines in the second number of conductor line openings using electroless plating;

depositing a third seed layer on the first level of conductor lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a third number of via holes opening to the third seed layer; and

forming a second level of copper vias in the third number of via holes using electroless plating.

21. (Previously Presented) The method of claim 20, wherein the method further comprises:

depositing a fourth seed layer on the second level of copper vias and third photoresist layer;

patterning a fourth photoresist layer over the fourth seed layer to define a fourth number of conductor line openings to the fourth seed layer; and

forming a second level of conductor lines in the fourth number of conductor line openings using electroless plating.

22. (Original) The method of claim 21, wherein depositing the first seed layer includes depositing a first seed layer having a discontinuous island structure.

23. (Original) The method of claim 22, wherein depositing a first seed layer having a discontinuous island structure includes depositing a discontinuous island structure of Palladium (Pd) or Copper (Cu).

24. (Previously Presented) The method of claim 21, wherein forming a first level of copper vias in the third number of via holes using electroless plating includes forming the third number of copper vias on the seed layer but not on the first photoresist layer.

25. (Original) The method of claim 21, wherein depositing a first seed layer includes depositing a first seed layer having a thickness of less than 15 nanometers (nm).

26. (Original) The method of claim 21, wherein depositing the first seed layer includes depositing the first seed layer using a physical vapor deposition process.

27. (Original) The method of claim 21, wherein patterning a second photoresist layer over the second seed layer includes patterning a second photoresist layer having a thickness which is less than a thickness of the first photoresist layer.

28. (Currently Amended) A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a semiconductor substrate using a physical vapor deposition process;

patterning a first photoresist layer over the first seed layer to define a first number of via holes opening to the first seed layer;

forming a first level of copper vias in the first number of via holes using electroless plating to a top surface of the first photoresist layer;

depositing a second seed layer on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a second number of conductor line openings to the second seed layer;

forming a first level of copper lines in the second number of conductor line openings using electroless plating;

depositing a third seed layer on the first level of copper lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a third number of via holes opening to the third seed layer;

forming a second level of copper vias in the third number of via holes using electroless plating; and

removing the first, second, and third photoresist layers using oxygen plasma etching.

29. (Original) The method of claim 28, wherein depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate using a physical vapor deposition process includes using an evaporation deposition technique.

30. (Original) The method of claim 28, wherein removing the first, second, and third photoresist layers using oxygen plasma etching includes removing the first, second, and third seed layers.

31. (Original) The method of claim 28, wherein depositing a second and a third seed layer includes depositing a second and third seed layer having a discontinuous island structure.

32. (Original) The method of claim 31, wherein depositing a second and a third seed layer having a discontinuous island structure includes depositing a second and a third seed layer using a sputtering deposition technique.

33. (Original) The method of claim 32, wherein depositing a second and a third seed layer includes depositing a second and a third seed layer having a thickness of less than 15 nanometers (nm).

34. (Previously Presented) A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a semiconductor substrate;

patterning a first photoresist layer over the first seed layer to define a first number of via holes opening to the first seed layer;

forming a first level of copper vias in the first number of via holes using electroless plating;

depositing a second seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a second number of conductor line openings to the second seed layer;

forming a first level of copper lines in the second number of conductor line openings using electroless plating;

depositing a third seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the first level of copper lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a third number of via holes opening to the third seed layer; and

forming a second level of copper vias in the third number of via holes using electroless plating;

depositing a fourth seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the second level of copper vias and third photoresist layer;

patterning a fourth photoresist layer over the fourth seed layer to define a fourth number of conductor line openings to the fourth seed layer; and

forming a second level of copper lines in the fourth number of conductor line openings using electroless plating.

35. (Original) The method of claim 34, wherein the depositing the first, second, third, and fourth seed layers includes depositing a first, second, third, and fourth seed layer having a discontinuous island structure.

36. (Original) The method of claim 35, wherein depositing a first, second, third, and fourth seed layer having a discontinuous island structure includes depositing a first, second, third, and fourth seed layer using a sputtering deposition technique.

37. (Original) The method of claim 36, wherein depositing a first, second, third, and fourth seed layer having a discontinuous island structure includes depositing a first, second, third, and fourth seed layer having thickness of less than 10 nanometers (nm).

38. (Original) The method of claim 34, wherein the method further includes removing the first, second, third, and fourth photoresist layers using an oxygen plasma etching.

39. (Original) The method of claim 38, wherein removing the first, second, third, and fourth photoresist layers using an oxygen plasma etching includes removing the first, second, third, and fourth seed layers.

40. (Previously Presented) The method of claim 39, wherein the further includes forming a thin diffusion barrier on the first number of via holes and on the third number of via holes and on the first level and the second level of copper lines.

41. (Original) The method of claim 40, wherein forming a thin diffusion barrier includes forming a thin diffusion barrier of Tungsten Silicon Nitride (WSixNy) having a thickness of less than 8 nanometers (nm).

42. (Original) The method of claim 41, wherein forming a thin diffusion barrier of Tungsten Silicon Nitride (WSixNy) having a thickness of less than 8 nanometers (nm) includes forming a graded composition of WSix, where x varies from 2.0 to 2.5, and nitriding the graded composition of WSix.

43-64. (Canceled)

65. (Previously Presented) The method of claim 7, wherein depositing a seed layer includes forming a discontinuous seed layer having island structures with the island structures having a thickness in a range of 3 to 10 nanometers.